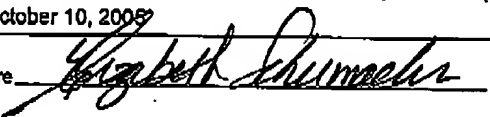
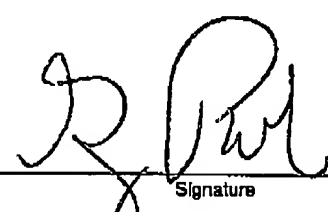


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<b>PRE-APPEAL BRIEF REQUEST FOR REVIEW</b>		Docket Number (Optional) 01-035	
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Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.  This request is being filed with a notice of appeal.  The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/86) <input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>44,995</u> <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____		 Signature Greg H. Parker Typed or printed name (972) 480-8800 Telephone number October 10, 2005 Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
<input checked="" type="checkbox"/> *Total of <u>1</u> forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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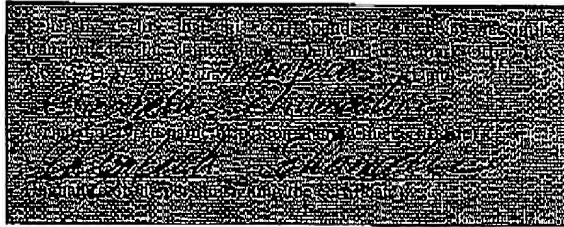
OCT 10 2005

ATTORNEY DOCKET NO. LSIL 01-035

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Theodore Vaida, *et al.*  
Serial No.: 09/851,181  
Filed: May 8, 2001  
Title: APPLICATION SPECIFIC INTEGRATED CIRCUIT HAVING A  
PROGRAMMABLE LOGIC CORE AND A METHOD OF OPERATION  
THEREOF  
Grp./A.U.: 2661  
Examiner: Phan, Tri. H.  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450



Sir:

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

The Applicants have carefully considered this application in connection with the Examiner's Final Rejection mailed July 15, 2005, and respectfully request a pre-appeal brief review of this application in view of the following remarks.

**REMARKS/ARGUMENTS**

The Applicants originally submitted Claims 1-42 in the application. Previously, the Applicants amended Claims 6, 15, 20-21, 30 and 34-35. Accordingly, Claims 1-42 are currently pending in the application.

**I. Rejection of Claims 1, 3, 5, 9-11, 13-17, 19, 23-25, 27-29, 31, 33, 37-39 and 41-42 under 35 U.S.C. §103**

The Examiner has rejected Claims 1, 3, 5, 9-11, 13-17, 19, 23-25, 27-29, 31, 33, 37-39 and 41-42 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,363,444 to Platko, *et al.* ("Platko") in view of U.S. Patent No. 4,969,121 to Chan, *et al.* ("Chan"). Each of Claims 1, 15 and 29 includes, in one form or another, an application specific integrated circuit (ASIC) that includes a programmable logic core. Specifically, independent Claims 1 and 29 outwardly require that the ASIC include the programmable logic core, wherein independent Claim 15 claims a method for operating an ASIC including a programmable logic core. Both Platko and Chan fail to teach or suggest this ASIC including a programmable logic core.

Platko is directed to a slave processor to slave memory data transfer with master processor writing address to slave memory and providing control input to slave processor and slave memory. (Title). Platko teaches that an ASIC 16, which is delineated by a box, is coupled to a serial EEPROM 26 via a bus between the serial EEPROM 26 and an EEPROM interface 58. The Examiner argues that the EEPROM 26 of Platko is inherently a programmable logic core, and thus Platko teaches or suggests an ASIC containing a programmable logic core. The Examiner's analysis of Platko, however, is inherently flawed (i.e., clearly erroneous). Specifically, the EEPROM 26 of Platko is not part of its ASIC 26, but is a stand-alone structure coupled to the ASIC 26 via the bus between the EEPROM 26 and the EEPROM interface 58, as is illustrated by the EEPROM 26 being outside of the box delineating the boundaries of the ASIC 16. Accordingly, Platko fails to disclose the element that the ASIC contains a programmable logic core. Moreover, Platko fails to suggest such an element because Platko requires that the EEPROM interface 58 be located within the ASIC to accommodate the standalone EEPROM 26. Thus, Platko fails to teach or suggest this element. The Examiner is clearly erroneous in arguing that Platko teaches or suggests this element.

Additionally, one skilled in the art would not be motivated to move the EEPROM 26 (which is located outside of the ASIC 16) within the ASIC 16 to form at least a portion thereof, because to do so would make the EEPROM interface 58 of no use. Namely, Platko has taken specific steps to place the EEPROM interface 58 in the ASIC 16 such that the external serial EEPROM 26 could be connected thereto. Removing such an EEPROM interface 58 and including the serial EEPROM 26 within the ASIC 16 would be non-obvious in view of the EEPROM interface 58 requirements. The only person that might take the serial EEPROM 26 of Platko, completely disregard the EEPROM interface 58 teaching, and move it within the ASIC 16, would be a person using the present invention as a blueprint to reconstruct the claimed invention. As the Review Panel is well aware, such non-obvious modifications based upon hindsight are not allowed.

Chan also fails to teach or suggest the claimed element that the ASIC contains a programmable logic core. The Examiner is offering Chan for the sole proposition that the programmable logic core has an array of dynamically configurable arithmetic logic units. Notwithstanding the merits of the Examiner's proposition, Chan further fails to teach or suggest the claimed element that the ASIC contains a programmable logic core. A teaching or suggestion of a programmable logic core having an array of dynamically configurable arithmetic logic units is dissimilar to a teaching or suggestion that an ASIC contain the programmable logic core, as currently claimed.

Thus, Platko, individually or in combination with Chan, fails to teach or suggest the invention recited in independent Claims 1, 15 and 29 and their dependent claims, when considered as a whole. Accordingly, these references fail to establish a *prima facie* case of obvious with respect to

these claims. Claims 1, 3, 5, 9-11, 13-17, 19, 23-25, 27-29, 31, 33, 37-39 and 41-42 are therefore not obvious in view of Platko and Chan.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1, 3, 5, 9-11, 13-17, 19, 23-25, 27-29, 31, 33, 37-39 and 41-42 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Review Panel to remove the rejection of independent Claims 1, 15 and 29 and the Claims dependent thereon.

## II. Conclusion

In view of the foregoing remarks, the Applicant sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-42.

The Applicant requests the Reviewers to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, PC

  
Greg H. Barker  
Registration No. 44,995

Dated: 10-10-05

P.O. Box 832570  
Richardson, Texas 75083  
(972) 480-8800